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PATENT & TRADEMARK OFFICE

PATENT APPLICATION

ATTORNEY DOCKET NO. 10008009-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Padmanabha I. VENKITAKRISHNAN, et al. **Confirmation No.:** 8711

Application No.: 09/916,598 **Examiner:** Knoll, C. H.

Filing Date: 07/26/01 **Group Art Unit:** 2112

Title: A CACHE COHERENT SPLIT TRANSACTION MEMORY BUS ARCHITECTURE AND PROTOCOL FOR A MULTI PROCESSOR CHIP

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TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **09/26/05**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( ) one month $120.00
( ) two months $450.00
( ) three months $1020.00
( ) four months $1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Rev 12/04 (Aplbrief)

Respectfully submitted,

Padmanabha I. VENKITAKRISHNAN, et

By ____________

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AP-
IPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Venkitakrishnan et al.	Patent Application	
Serial No.:	09/916,598	Group Art Unit:	2112
Filed:	July 26, 2001	Examiner:	Knoll, C.

For: A CACHE COHERENT SPLIT TRANSACTION MEMORY BUS ARCHITECTURE AND PROTOCOL FOR A MULTI PROCESSOR CHIP

Appeal Brief

Table of Contents

Real Party in Interest

The Appellant Hewlett-Packard Company is the real party in interest.

Related Appeals and Interferences

There are no related appeals or interferences known to the Appellant.

Status of Claims

Claims 1-20 are pending. Claims 1-20 are rejected. Claims 1-4, 7 and 9 are rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli et al. (U.S. Patent No. 6,587,926). Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Bitar et al. (U.S. Patent No. 6,418,460). Claims 10-13, 16 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546). Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322). Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546) and further in view of Arimilli et al. (U.S. Patent No. 6,571,322).

Status of Amendments

No amendments were filed after the issuance of the final rejection mailed on June 2, 2005.

Summary of Claimed Subject Matter

Independent Claim 1 details a cache coherent multiple processor integrated circuit. In the Claim 1 embodiment, the cache coherent multiple processor integrated circuit comprises a plurality of processor units, and embedded RAM unit and a cache coherent bus. The bus is configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

Corresponding to the embodiment detailed in Claim 1, a cache coherent multiple processor integrated circuit is discussed in Appellants' specification beginning at page 9, line 4, where Figure 1 is described. Figure 1 includes a diagram of a cache coherent multiple processor integrated circuit that is described in Appellants' specification. Referring to Figure 1, the diagram shows structures that are a part of the embodiment of the invention that is set forth in Claim 1.

Independent Claim 10 details an integrated circuit device. In the Claim 10 embodiment, the integrated circuit device comprises a plurality of processor units, an embedded RAM unit and a cache coherent bus. The bus is configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

Corresponding to the embodiment detailed in Claim 10, an integrated circuit device is discussed in Appellants' specification beginning at page 9, line 4, where Figure 1 is described. Figure 1 includes a diagram of an integrated circuit device that is described in Appellants' specification. Referring to Figure 1, the diagram shows structures that are a part of the embodiment of the invention that is set forth in Claim 10.

Independent Claim 19 details a portable hand held electronic device. In the Claim 19 embodiment, the hand held electronic device comprises a plurality of processor units, a plurality of cache units, an embedded DRAM unit and a 256 bit cache coherent bus. The bus is configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

Corresponding to the embodiment detailed in Claim 19, an integrated circuit device is discussed in Appellants' specification beginning at page 9, line 4, where Figure 1 is described. Figure 1 includes a diagram of an hand held electronic device that is described in Appellants' specification. Referring to Figure 1, the diagram shows structures that are a part of the embodiment of the invention that is set forth in Claim 19.

<u>Grounds Of Rejection To Be Reviewed On Appeal</u>

Claims 1-4, 7 and 9 are rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli et al. (U.S. Patent No. 6,587,926).

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322).

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,587,926).

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Bitar et al. (U.S. Patent No. 6,418,460).

Claims 10-13, 16 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546).

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322).

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,587,926).

Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,587,926).

Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546) and further in view of Arimilli et al. (U.S. Patent No. 6,571,322).

Argument

The rejection of Claims 1-4, 7 and 9 under 35 U.S.C. § 102(e) as being anticipated by Arimilli et al. (U.S. Patent No. 6,587,926).

A. Scope and Content of the Cited Reference (Arimilli et al. (U.S. Patent No. 6,587,926)

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

B. Differences Between Arimilli et al. and the claimed Invention

The cited prior art reference, Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag

builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

Arimilli et al. does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1. It should be appreciated that the Arimilli et al. reference is concerned with the management of data access transactions within a data storage system and not with providing cache coherency between cache units for a processor and an embedded RAM unit as claimed.

In contrast to the invention embodiments set forth in Appellants' claims, in the system that is disclosed by Arimilli et al. snooping is performed by storage devices (or internal processors thereof) and third party transactors (see column 9, lines 35-40). Importantly, in the system that is disclosed by Arimilli et al. there is no teaching or suggestion that the snooping is for ensuring cache coherency between cache units for processors and an embedded RAM unit as is recited in Claim 1. Moreover, Arimilli et al. teaches sharply away from these claimed features of the invention embodiments as Arimilli et al. shows in Figure 5 that in his disclosed system a snoop request is made when a coherency update is <u>not needed</u> (see step 510).

Indeed, nowhere in the Arimilli et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units <u>that enable the processor units themselves</u> to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim

1. Consequently, Arimilli et al. does not anticipate or render obvious the embodiment of the Appellants' invention set forth in Claim 1.

In order to anticipate a claim a reference must teach each and every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed Cir. 1987). It is clear from the discussion above that "each and every element" of Claim 1 is in fact not described by the Arimilli et al. reference. More specifically, Arimilli et al. does not "either expressly or inherently" show or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1.

Accordingly, Appellants respectfully submit that Arimilli et al. does not anticipate or render obvious the embodiments of the Appellants' invention as are recited in Claims 2-4, 7 and 9 as these Claims are dependent on Claim 1. Therefore, these Claims are rejected improperly under 35 U.S.C. 102(e) as these Claims are dependent on allowable Claim 1.

Appellant respectfully submits that an incredible degree of hindsight has been employed in combining the numerous cited references for the purpose of rejecting Appellant's Claims as proper motivation to combine the cited references is lacking. It should be appreciated that even if proper motivation to combine the references were indeed present, as discussed above, the cited combination nonetheless would not teach or suggest the claimed invention since the sum total of the information taught or

suggested by the referenced subject matter is insufficient to meet all of the limitations of the claimed invention.

The rejection of Claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322).

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No. 6,587,926] in view of Arimilli et al. [U.S. Patent No. 6,571,322])

The Arimilli et al. (U.S. Patent No. 6,587,926) reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Arimilli et al. (U.S. Patent No. 6,571,322) reference pertains to a multiprocessor computer system with a sectored cache line mechanism for cache intervention. More specifically, Arimilli et al. discloses a method of maintaining coherency in a multiprocessor computer system wherin each processing unit's cache has sectored cache lines.

B. Differences Between Arimilli et al. and Arimilli et al. and the Claimed Invention

Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) that will remedy the deficiencies of Arimilli et al. (U.S. Patent No. 6,587,926) outlined above. More specifically, Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a

cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1 (from which Claim 5 depends).

Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention. Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 1 (from which Claim 5 depends). Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of Appellants' invention as set forth in Claim 1 (from which Claim 5 depends). Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 5 dependent on Claim 1 and that Claim 5 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

<u>The rejection of Claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,587,926)</u>

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No.

6,587,926] in view of Miller et al. [U.S. Patent No. 6,587,926])

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Miller et al. reference pertains to a system and method for terminating lock step sequences in a multiprocessor system. More specifically, Miller et al. discloses a control circuit that perturbs a lock step sequence of memory requests received from processors of the multiprocessor system.

B. Differences Between Arimilli et al. and Miller et al. and the Claimed Invention

Miller et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al outlined above. More specifically, Miller et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1 (from which Claim 6 depends).

Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems. Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the

cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 1 (from which Claim 6 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the embodiment of the Appellants' invention as set forth in Claim 1 (from which Claim 6 depends). Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 6 dependent on Claim 1 and that Claim 6 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

<u>The rejection of Claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Bitar et al. (U.S. Patent No. 6,418,460).</u>

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No. 6,587,926] in view of Bitar et al. [U.S. Patent No. 6,418,460])

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Bitar et al. reference pertains to a system and method for finding preemptive threads in a multi-threaded application. More specifically, Bitar et al. discloses a system and method for inexpensively detecting preempted execution entities such as threads without kernel involvement.

B. Differences Between Bitar et al. and the Claimed Invention

Bitar et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Bitar et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 1 (from which Claim 8 depends).

Bitar et al. only shows a system and method for finding preempted threads in a multi-threaded application. Nowhere in the Bitar et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 1 (from which Claim 8 depends). Consequently, Arimilli et al. either alone or in combination with Bitar et al., does not anticipate or render obvious the embodiment of the Appellants' invention as set forth in Claim 1 (from which Claim 8 depends). Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Bitar et al. (U.S. Patent No. 6,418,460) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 8 dependent on Claim 1 and that Claim 8 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

The rejection of Claims 10-13, 16 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546).

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No. 6,587,926] in view of Sherburne [U.S. Patent Application Publication No. 2002/0184546])

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Sherburne et al. reference pertains to method and device for modifying the memory contents of a memory. More specifically, Sherburne et al. discloses a low power reconfigurable processor core that includes one or more processing units, where each unit has a clock input that controls the performance of the unit and a controller that has a plurality of clock outputs each coupled to the clock inputs of the processing units. The controller varies the clock frequency of each processing unit to optimize power consumption and processing power for a task.

B. Differences Between Sherburne et al. and the Claimed Invention

Sherburne does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Sherburne does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands

from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 10. Sherburne only shows a method and device for modifying the contents of memory.

Nowhere in the Sherburne et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 10. Consequently, Arimilli et al. either alone or in combination with Sherburne does not anticipate or render obvious the embodiment of the Appellants' invention as set forth in Claim 10. Accordingly, Appellants respectfully submit that Arimilli et al. alone or in combination with Sherburne does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claims 11-13, 16 and 18 dependent on Claim 10 and that these Claims overcome the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

<u>The rejection of Claim 14 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Arimilli et al. (U.S. Patent No. 6,571,322).</u>

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No. 6,587,926] in view of Arimilli et al. [U.S. Patent No. 6,571,322])

The Arimilli et al. (U.S. Patent No. 6,587,926) reference pertains to the management of data access transactions within a hierarchical data storage system.

More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Arimilli et al. (U.S. Patent No. 6,571,322) reference pertains to a multiprocessor computer system with a sectored cache line mechanism for cache intervention. More specifically, Arimilli et al. discloses a method of maintaining coherency in a multiprocessor computer system wherin each processing unit's cache has sectored cache lines.

B. Differences Between Arimilli et al. and the Claimed Invention

Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) that remedies the deficiencies of Arimilli et al. (U.S. Patent No. 6,587,926) outlined above. More specifically, Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 10 (from which Claim 14 depends). Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention.

Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as

is recited in Claim 10 (from which Claim 14 depends). Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the Appellants' invention as set forth in Claim 10 (from which Claim 14 depends). Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 14 dependent on Claim 10 and that Claim 14 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

<u>The rejection of Claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al. (U.S. Patent No. 6,560,682</u>

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No. 6,587,926] in view of Miller et al. [U.S. Patent No. 6,560,682])

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Miller et al. reference pertains to a system and method for terminating lock step sequences in a multiprocessor system. More specifically, Miller et al.

discloses a control circuit that perturbs a lock step sequence of memory requests received from processors of the multiprocessor system.

B. Differences Between Miller et al. and the Claimed Invention

Miller et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Miller et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 10 (from which Claim 15 depends). Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems.

Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 10 (from which Claim 15 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the embodiment of the Appellants' invention as set forth in Claim 10 (from which Claim 15 depends). Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 15 dependent on Claim 10 and that Claim 15 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

The rejection of Claim 17 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Miller et al.

A. Scope and Content of the Cited References Arimilli et al. (U.S. Patent No. 6,560,682) in view of Miller et al. (U.S. Patent No. 6,560,682)

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Miller et al. reference pertains to a system and method for terminating lock step sequences in a multiprocessor system. More specifically, Miller et al. discloses a control circuit that perturbs a lock step sequence of memory requests received from processors of the multiprocessor system.

B. Differences Between Miller et al. and the Claimed Invention

Miller et al. does not teach or suggest a modification of Arimilli et al. that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Miller et al. does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit"

as is recited in Claim 10 (from which Claim 17 depends). Miller et al. only shows a system and method for terminating lock-step sequences in multiprocessor systems.

Nowhere in the Miller et al. reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in Claim 10 (from which Claim 17 depends). Consequently, Arimilli et al. either alone or in combination with Miller et al. does not anticipate or render obvious the embodiment of the Appellants' invention as set forth in Claim 10 (from which Claim 17 depends). Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Miller et al. (U.S. Patent No. 6,560,682) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 17 dependent on Claim 10 and that Claim 17 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

<u>The rejection of Claims 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,587,926) in view of Sherburne (U.S. Patent Application Publication No. 2002/0184546) and further in view of Arimilli et al. (U.S. Patent No. 6,571,322).</u>

A. Scope and Content of the Cited References (Arimilli et al. [U.S. Patent No. 6,587,926] in view of Sherburne [U.S. Patent Application Publication No. 2002/0184546] and further in view of Arimilli et al. [U.S. Patent No. 6,571,322]).

The Arimilli et al. reference pertains to the management of data access transactions within a hierarchical data storage system. More specifically, the Arimilli et al. reference discloses the use of incremental tag builds in a hierarchical data storage system as a means of managing data access within a hierarchical data storage system.

The Sherburne et al. reference pertains to method and device for modifying the memory contents of a memory. More specifically, Sherburne et al. discloses a low power reconfigurable processor core that includes one or more processing units, where each unit has a clock input that controls the performance of the unit and a controller that has a plurality of clock outputs each coupled to the clock inputs of the processing units. The controller varies the clock frequency of each processing unit to optimize power consumption and processing power for a task.

The Arimilli et al. reference pertains to a multiprocessor computer system with a sectored cache line mechanism for cache intervention. More specifically, Arimilli et al. discloses a method of maintaining coherency in a multiprocessor computer system wherin each processing unit's cache has sectored cache lines.

B. Differences Between Arimilli et al., Sherburne et al. and Arimilli et al. and the Claimed Invention

Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a modification of Arimilli et al. (U.S. Patent No. 6,587,926) and Sherburne (U.S. Patent Application Publication No. 2002/0184546) that remedies the deficiencies of Arimilli et al. outlined above. More specifically, Arimilli et al. (U.S. Patent No. 6,571,322) does not teach or suggest a cache coherent multiple processor integrated circuit that includes a bus configured to "provide cache coherent snooping commands from the

processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit" as is recited in Claim 19. Arimilli et al. (U.S. Patent No. 6,571,322) only shows a multiprocessor computer system with a mechanism for cache intervention.

Nowhere in the Arimilli et al. (U.S. Patent No. 6,571,322) reference is a bus that is configured to provide cache coherent snooping commands from processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processor units and an embedded RAM unit taught or suggested as is recited in claim 19. Consequently, Arimilli et al. (U.S. Patent No. 6,587,926) either alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) and Sherburne (U.S. Patent Application Publication No. 2002/0184546) does not anticipate or render obvious the embodiment of the Appellants invention as set forth in Claim 19. Accordingly, Appellants respectfully submit that Arimilli et al. (U.S. Patent No. 6,587,926) alone or in combination with Arimilli et al. (U.S. Patent No. 6,571,322) does not anticipate or render obvious the embodiment of the present claimed invention as is recited in Claim 20 dependent on Claim 19 and that Claim 20 overcomes the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Conclusions

Appellants believe that pending Claims 1-20 are patentable over the cited references taken either alone or in combination. Accordingly, Appellants respectfully request that the rejection of these claims be reversed.

Respectfully submitted,

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Appendix - Clean Copy of Claims

1. A cache coherent multiple processor integrated circuit, comprising:

a plurality of processor units;

a plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded RAM unit for storing instructions and data for the processor units;

a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

2. The circuit of Claim 1, further comprising an input output unit coupled to the bus to provide input and output transactions for the processor units.

3. The circuit of Claim 1, wherein the bus is configured to provide split transactions for the processor units coupled to the bus.

4. The circuit of Claim 1, wherein the bus is configured to transfer an entire cache line for the cache units of the processor units.

5. The circuit of Claim 1, wherein the bus is 256 bits wide.

6. The circuit of Claim 1, wherein the RAM unit is an embedded DRAM core.

7. The circuit of Claim 1, wherein the bus is configured to support a symmetric multiprocessing method for the plurality of processor units.

8. The circuit of Claim 1, wherein the processor units are compatible with a version of a MIPS processor core.

9. The circuit of Claim 1, wherein the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit.

10. An integrated circuit device, comprising:

an integrated circuit die; and

a power supply coupled to the integrated circuit die, wherein the integrated circuit die includes therein:

a plurality of processor units;

a plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded RAM unit for storing instructions and data for the processor units;

a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded RAM unit.

11. The circuit of Claim 10, further comprising an input output unit coupled to the bus to provide input and output transactions for the processor

units.

12. The circuit of Claim 10, wherein the bus is configured to provide split transactions for the processor units coupled to the bus.

13. The circuit of Claim 10, wherein the bus is configured to transfer an entire cache line for the cache units of the processor units.

14. The circuit of Claim 10, wherein the bus is 256 bits wide.

15. The circuit of Claim 10, wherein the RAM unit is an embedded DRAM core.

16. The circuit of Claim 10, wherein the bus is configured to support a symmetric multiprocessing method for the plurality of processor units.

17. The circuit of Claim 10, wherein the processor units are compatible with a version of a MIPS processor core.

18. The circuit of Claim 10, wherein the processor units are configured to provide read data via the bus when the read data is stored within a respective cache unit.

19. A portable hand-held electronic device, comprising:

an integrated circuit die; and

a power supply coupled to the integrated circuit die, wherein the

integrated circuit die includes therein:

a plurality of processor units;

plurality of cache units, one of the cache units provided for each one of the processor units;

an embedded DRAM core unit for storing instructions and data for the processor units;

a 256 bit cache coherent bus coupled to the processor units and the embedded DRAM core unit, the bus configured to provide cache coherent snooping commands from the processor units that enable the processor units themselves to ensure cache coherency between the cache units for the processors and the embedded DRAM core unit.

20. The circuit of Claim 19, wherein the bus is configured to provide split transactions for the processor units coupled to the bus.